DOCKET NO.: 200300032-2

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

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| In re patent application of: | § | |
| | § | |
| Richard Adkisson et al. | § | Confirmation No.: 7891 |
| | § | |
| Application No.: 10/625,291 | § | Art Unit: 2616 |
| | § | |
| Filed: July 23, 2003 | § | Examiner: Sai Ming Chan |

For: SYSTEM AND METHOD FOR EFFECTUATING THE TRANSFER OF DATA BLOCKS INCLUDING A HEADER BLOCK ACROSS A CLOCK BOUNDARY

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

**APPEAL BRIEF UNDER 37 C.F.R. §41.37**

Pursuant to 37 C.F.R. §41.37, Applicant (hereinafter "Appellant") hereby submits this appeal brief in the above-captioned patent application within the requisite time from the date of filing of the Notice of Appeal which is filed herewith.

This appeal is from the decision of Examiner Sai Ming Chan, Art Unit 2616, rejecting all pending claims 1-16 in the present patent application, as set forth in the Final Office Action dated August 20, 2008.

## I. REAL PARTY IN INTEREST

The real party in interest of the present patent application is Hewlett-Packard Development Company, a Texas Limited Liability Partnership having its principal place of business in Houston, Texas.

## II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any other prior and/or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by or otherwise have a bearing on the Board's decision in this pending appeal.

## III. STATUS OF CLAIMS

Claims 1-16 are currently pending, of which claims 1, 10 and 13 are in independent form.

Claims 1-16 stand rejected as follows:

Claims 1, 3-7, 10, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Shin* in view of *Jones* and *Arimilli*.

Claims 2, 8, 9, 11, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Shin* in view of *Jones*, *Arimilli* and *Naumann*.

Claims 1-16 are appealed.

## IV. STATUS OF AMENDMENTS

Set forth below is a synopsis of the chronology with respect to claim amendments:

A First Office Action on the merits was mailed on August 7, 2007 rejecting pending base claims 1, 10 and 13 under 35 U.S.C. §103(a) over *Shin* in view of *Locker*.

Appellant filed a Response on November 6, 2007 in which no claim amendments were made and arguments were presented.

A Second Office Action was mailed on February 7, 2008 in which pending base claims 1, 10 and 13 were rejected under 35 U.S.C. §103(a) over *Shin* in view of *Locker* and *Arimilli*.

Appellant filed a Response on May 6, 2008 in which pending base claims 1, 10 and 13 were amended and arguments were presented.

A Final Office Action was mailed on August 20, 2008 in which pending base claims 1, 10 and 13 were rejected under 35 U.S.C. §103(a) over *Shin* in view of *Jones* and *Arimilli*.

Appellant is filing a Notice of Appeal herewith in response.

A copy of the claims related to this appeal is attached hereto as an Appendix.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

A concise explanation of the subject matter defined in each of the independent claims is set forth in this Section, including appropriate references to the specification, e.g., by page and line number, reference numerals in drawings, etc. These specific references are examples of particular elements of the drawings for certain embodiments of the claimed invention, and the claims are not limited solely to the elements corresponding to the applied reference numerals.

Independent claim 1 is directed to an embodiment of a system for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, (see, e.g., system 200 in the functional block diagram of FIGURE 2 as well as related description in the specification at Paragraphs [0018] to [0025]) wherein the first clock domain is operable with a first clock signal and the second clock domain is operable with a second clock signal, the first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1 (see, e.g., slow clock domain

in the upper portion of FIG. 2 and fast clock domain in the lower portion of FIG. 2). The claimed embodiment comprises a first circuit portion (e.g., 204) for providing data blocks including header block to a second circuit portion (e.g., 208). The system also comprises control logic (e.g., 222) associated with the second circuit portion (e.g., 208) for processing the header block and generating, in response to the header block, a hint signal (e.g., 244) that gives advance notification of a possible data transfer operation, the hint signal being operable to be transferred via a synchronizer (e.g., 226) at least one data cycle prior to the transfer of the data blocks to a third circuit portion (e.g., 240). The system further comprises a control block (e.g., 242) associated with the third circuit portion (e.g., 240), the control block (e.g., 242) operating responsive to the hint signal (e.g., 244) to generate data transfer control signals for controlling the third circuit portion (e.g., 240) in order to control output of the data blocks in a particular ordered grouping. The first circuit portion (e.g., 204), the second circuit portion (e.g., 208) and the control logic (e.g., 222) are disposed in the first clock domain (e.g., fast clock domain) and the third circuit portion (e.g., 240) and the control block (e.g., 242) are disposed in the second clock domain (e.g., slow clock domain).

Independent claim 10 is directed to an embodiment of a method for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain (see, e.g., the flowchart of FIG. 4 as well as related description in the specification at Paragraph [0027] et seq.), wherein the first clock domain is operable with a first clock signal (CLK1) and the second clock domain is operable with a second clock signal (CLK2). The method comprises processing (element 400) a header block associated with data blocks that are to be sent from the first clock domain to the second clock domain via a synchronizer, generating a hint signal that gives advance notification of a possible data transfer operation in response to the header block and positioning (element 402) the hint signal at least one cycle prior to the location of the data blocks, with processing the header block and the generating the hint signal being performed in the first clock domain. The method further comprises transmitting (element 404) the hint signal to a control block in the second clock domain, thereby indicating that the data blocks may be sent to receive circuitry in the second clock domain, and generating (element 406) appropriate control signals based on the hint signal for controlling output of the data blocks in a particular ordered grouping.

Independent claim 13 is directed to an embodiment of a computer system having circuitry for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain (see, e.g., system 200 in the functional block diagram of FIGURE 2 as well as related description in the specification at Paragraphs [0018] to [0025]), wherein the first clock domain is operable with a first clock signal (CLK1) and the second clock domain is operable with a second clock signal (CLK2), the first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1. The computer system comprises means for processing (e.g., 222) a header block associated with the data blocks to determine whether the data blocks may be sent from the first clock domain to the second clock domain via a synchronizer and means for generating (e.g., 222) a hint signal that gives advance notification of a possible data transfer operation in response to the header block. The hint signal (e.g., 244) is operable to be positioned at least one cycle prior to the possible location of the data blocks. Further, the means for processing (e.g., 222) a header block and the means for generating (e.g., 222) a hint signal are disposed in the first clock domain. The computer system further comprises means for transmitting (e.g., 226) the

hint signal to a control block (e.g., 242) in the second clock domain, thereby indicating that the data blocks may be sent to receive circuitry in the second clock domain. The control block (e.g., 242) generates appropriate control signals, based on the hint signal, for controlling output of the data blocks in a particular ordered grouping.

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 3-7, 10, 13, and 14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2004/0004975 to Shin et al. (hereinafter the *Shin* reference), in view of U.S. Patent Publication No. 2003/0204555 to Jones et al. (hereinafter the *Jones* reference) and U.S. Patent No 6,874,063 to Arimilli et al. (hereinafter the *Arimilli* reference).

B. Claims 2, 8, 9, 11, 12, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Shin* in view of *Jones*, *Arimilli* and U.S. Patent Publication No. 2004/0024946 to Naumann et al. (hereinafter the *Naumann* reference).

## VII. ARGUMENT

### A. Claims 1, 3-7, 10, 13 and 14 are not obvious over the combination of *Shin* with *Jones* and *Arimilli*.

If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985). The determination of "nonobviousness" is made after establishing the scope and content of prior art, the differences between the prior art and the claims at issue, and the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1 (1966). In addition, all limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 21 U.S.P.Q.2d 1031, 1034 (Fed Cir. 1994).

The Board should reverse the Examiner because the Examiner has not presented a *prima facie* case of unpatentablity and has not shown that all limitations of the claims are shown or suggested by the art relied on.

In connection with these §103(a) rejections, the Examiner has made the following determinations with respect to base claim 1:

Consider claim 1, Shin et al. clearly disclose and show a system for effectuating the transfer of data blocks including a header block (fig. 4 (410), fig. 5(500 header); paragraph 9 (header)) across a clock boundary (paragraph 0009 (transmitter's and receiver's clock domains)) between a first clock domain (paragraph 9 (transmitter's clock domain)) and a second clock domain (paragraph 9 (receiving device's local clock frequency)), wherein said first clock domain is operable with a first clock signal (paragraph 9 (transmitter's clock domain)) and said second clock domain is operable with a second clock signal (paragraph 9 (receiving device's local clock frequency)), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M>1(paragraph 73 (transmitter's frequency is faster than the receiver's (an overrun condition))), comprising:

a first circuit portion (fig. 2 (201 transmitter; fig. 3)) for providing said data blocks including said header block to a second circuit portion (fig. 2 (202 receiver; fig. 3));

control logic associated with said second circuit portion for processing said header block (fig.3; paragraphs 3 and 83 (control the transmission and reception of the symbols)), and a synchronizer (paragraph 0009 (send signal so that receiver can synchronize with the transmitter)).

However, Shin et al. do not specifically disclose the sending of hint signal across clock boundary.

In the same field of endeavor, Jones et al. clearly shows the sending of hint signal that gives advance notification of a possible data transfer operation (fig. 10 (724), paragraph 0129 (hints for transfer)), wherein the first circuit portion and second circuit portion and said control logic (fig. 7, paragraph 0122) are disposed in said first clock domain (fig. 10(724)) and said third circuit portion and said control block are disposed in said second clock domain (fig. 10 (726 (send hints to another digital processing system)), paragraph 0135).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught

by Shin et al., and incorporate the hint signal, as taught by Jones et al., so that appropriate element would be selected.

However, Shin et al., as modified by Jones, do not specifically disclose the ordering of data transfer.

In the same field of endeavor, Arimilli et al. clearly shows the ordering of data transfer (abstract (order bit for transmitting data in that order)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate hint signal, as taught by Jones et al., and ordering of data transfer, as taught by Arimilli, so that data transfer between two clock domains is done efficiently.

**The *Shin* reference**

The *Shin* reference is directed to a serial communications architecture for communicating between hosts and data store devices via a switching network. See Abstract. Data is transferred in *Shin* using a plesiosynchronous clocking technique, in which the transmitting and receiving devices have clocks with nominally the same clock frequency. In practice clock frequencies are not exactly the same but vary, for example, by 100 ppm. To compensate, the receiving device can use techniques that include an oversampling of the data by the receiving device to detect edge boundaries of the transmitted data, allowing the receiving device to vary the number of bits of data detected during an interval to compensate for the variations in frequency. In addition to

oversampling the data, the plesiochronous clocking technique uses the insertion and removal of symbols by the physical layer of a receiving communications node to compensate for the relatively small variations in clock frequency between the transmitter and receiver. See Paragraph [0010] and [0073].

**The *Jones* reference**

The *Jones* reference is directed to processing time related media data (e.g., a movie) for transmission to another system. *Jones* discloses that time related media can be stored in a number of formats used for content delivery, which differ depending on the focus of the file format. See Paragraph [0002]. When the media is transmitted to the network (e.g., the Internet), the media must be packetized into one of several transmission formats, which may be different from the delivery format in which the media is stored. One can packetize the media at transmission time or store the media in a packetized format, the former option requiring less storage space and the latter option requiring less processing at transmission. See Paragraphs [0042]-[0045]. *Jones* provides an improvement to these methods in which hints for packetizing a time related sequence of media data according to a given transmission protocol are created and stored, either with the media data or

separately. These hints are then used when the time related media data is transmitted using the given transmission protocol. By storing hints for different transmission protocols along with the basic presentation format, transmission of the file is facilitated in any transmission format for which hints have been stored. See Paragraphs [0065] and [0087].

**The *Arimilli* reference**

The *Arimilli* reference is directed to a method for informing a processor of a selected order of transmission of data to the processor. See Abstract. *Arimilli* appears to have been cited solely for the ordering this reference shows and does not appear to contribute further to the combination of references.

Appellant respectfully asserts that the combination of cited references does not disclose all of the limitations of the embodiments recited in the base claims. Appellant has identified at least the following deficiencies in the cited art:

**1) Claim 1 features a hint signal that gives advance notification of a possible data transfer operation, the hint signal being transferred at least one data cycle prior to the transfer of associated data blocks, which the cited art does not show.**

The Examiner has admitted that *Shin* does not disclose sending a hint signal across clock boundaries, but asserts that *Jones* sends a hint signal that gives advance notification of a possible data transfer operation and points for support to *Jones'* Paragraph [0129] and also to element 724 of FIG. 10, which is reproduced herein for convenience. Appellant submits that while this figure of *Jones* discloses the use of hints, the figure also discloses that the hints are for "packetizing a time related sequence of media data". Paragraph [0129] also discusses that the hints are used for packetizing the media data. Thus, the hints of *Jones* appear to be related to the transfer of data inasmuch as the hints are used to prepare the data for transmission. However, *Jones'* hints do not give advance

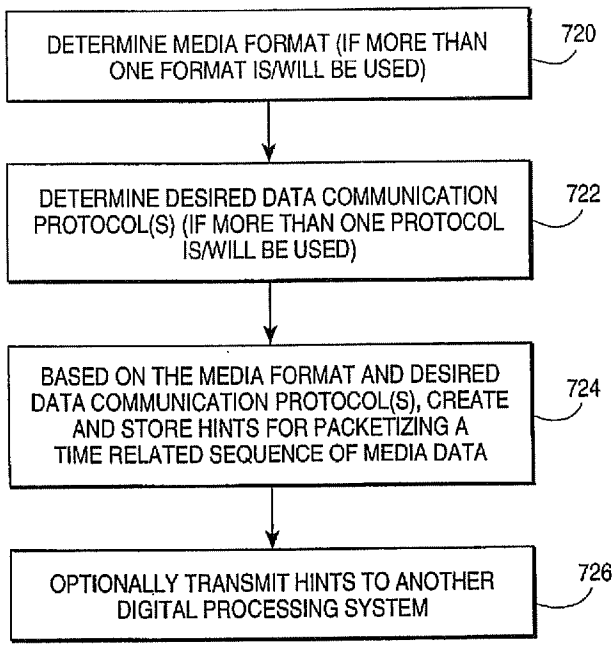


FIG. 10

notification of a possible data transfer, but provide information to be used prior to a data transfer. While one might conceivably argue that by their existence, the hints of *Jones* give notice that at some vague time in the future, there may be a data transfer operation that will use these hints, such a "hint" would not be useful in the system and method of the claimed embodiments and thus would not be used by one of ordinary skill in the art.

In order for a hint to be useful in the claimed method and system by giving advance notification of a possible data transfer, the hint should precede the data during transmission, i.e., the hint should be transferred at least one clock cycle prior to the transfer of associated data blocks, as is featured in the independent claims. *Jones* does not disclose that the hint is transferred prior to the transfer of associated data blocks.

*Jones* makes clear that transmission of the hints along with the media data is not necessary to the functioning of the hints and that when the receiving system does not intend to packetize the media for further transmission, sending the hints may be wasteful of bandwidth. See Paragraph [0081]. *Jones* does disclose, in FIG. 4, an example of the hints being transmitted along with the media data. However, as shown in this example, which is reproduced herein for convenience, the hints actually follow the media data

which is associated with them. See Paragraph [0084] and hint track sample 405, which contains a pointer that points to the associated media that precedes the hint.

As all of this discussion shows, *Jones* does not disclose or suggest a "hint signal that gives advance notification of a possible data transfer operation, said hint signal being operable to be transferred via a synchronizer at least one data cycle prior to the transfer of said data blocks", as is recited in claim 1.

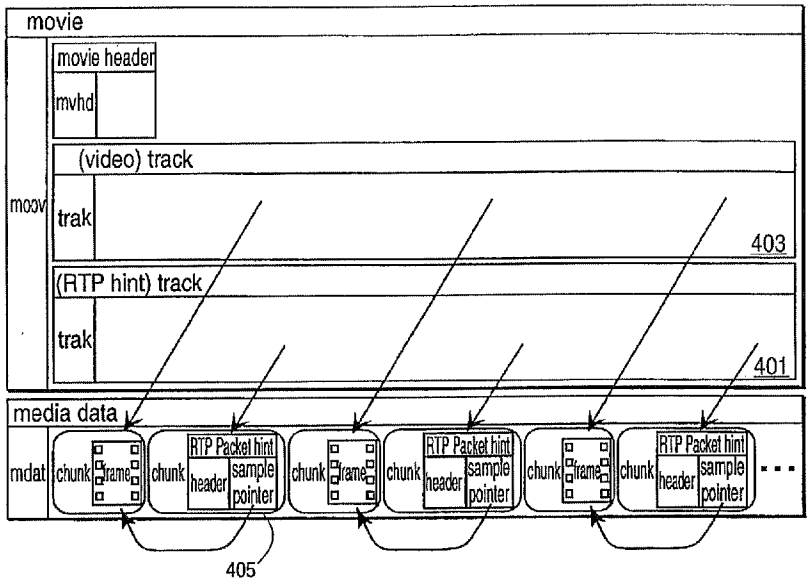


FIG. 4

**2) Claim 1 features control logic that generates the hint signal in response to the header block, which the cited art does not.**

The Examiner has read the claimed control logic for processing the header blocks on FIG. 3 and Paragraphs [0003] and [0083] of

*Shin*. FIG. 3 of *Shin*, which is reproduced herein for convenience, shows an embodiment of the physical layer 230 of *Shin's* communications architecture. Physical layer 230 includes transmitter 231, receiver 235, phase lock loop 301, and clock 302. Phase lock loop 301 provides a timing signal to the transmitter for the serial transmission of the symbols and provides multiple timing signals with different phases to the receiver for receiving serially transmitted data and symbols. Various received symbols can be recognized by the physical layer, which adjusts to the differences in speed between the transmitter and receiver by inserting or removing specific symbols from the data stream. See Paragraphs [0083]-[0084]. *Shin* does not appear to disclose or suggest the processing of header blocks in these excerpts or to suggest how processing downstream might be aided by hints created here. Although *Shin* discloses that the physical layer controls the transmission and reception of symbols, these symbols are separate

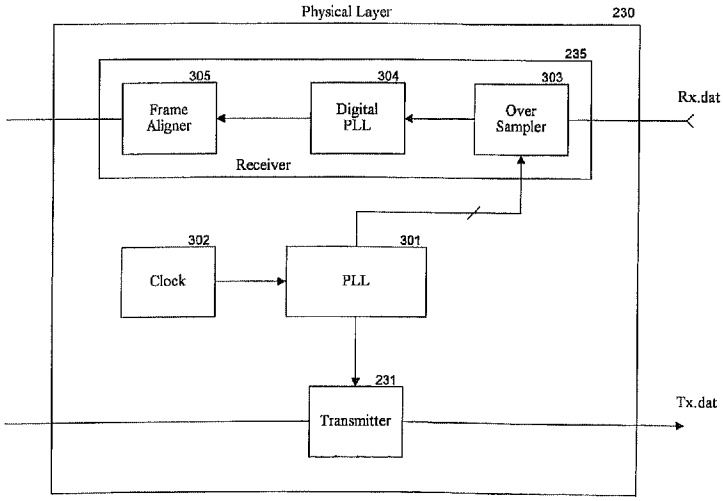


***Fig. 3***

and distinct from the headers that *Shin* discusses and to which the Examiner points. The symbols do not have the same information as a header block and are not used in the same way that a header block is used. Accordingly, *Shin* does not disclose "control logic associated with second circuit portion for processing said header block", as is recited in claim 1.

**3) Claim 1 features a control block that responds to the hint signal by generating control signals to control the data transfer, which the cited art does not.**

Claim 1 includes a recitation of "a control block associated with said third circuit portion ... [and] operating responsive to said hint signal to generate data transfer control signals for controlling said third circuit portion ... wherein ... said third circuit portion and said control block are disposed in said second clock domain." The Office Action does not point to any portion of *Shin* as showing the control block that responds to the hint signal by generating control signals. The only time that the recited control block is referenced in the Office Action is by pointing to FIG. 10, element 726, of *Jones*, in which the transmitting system optionally transmits hints to the receiving system. However, *Jones* does not disclose that the hints, when they are present in the transmission, are used to control the receiving system. The hints

of *Jones* are utilized only by the transmitting system and are not relevant to the receiving system, which is where the claimed control block exists. Accordingly, *Jones* does not disclose "a control block associated with said third circuit portion, said control block operating responsive to said hint signal to generate data transfer control signals for controlling said third circuit portion in order to control output of said data blocks", as is recited in claim 1.

For at least the foregoing reasons, Appellant respectfully submits that the Examiner has not presented a *prima facie* case of obviousness against base claim 1. Base claims 10 and 13 contain substantially corresponding elements and provide the same distinctions over the cited art. Accordingly, Appellant respectfully submits that pending base claims 1, 10 and 13, as well as the dependent claims that respectively depend therefrom, are allowable over the cited references.

**B. Claims 2, 8, 9, 11, 12, 15, and 16 are allowable over the cited references.**

Claims 2, 8, 9, 11, 12, 15, and 16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Shin* in view of *Jones*, *Arimilli* and *Naumann*.

As discussed above, the combination of *Shin*, *Jones* and *Arimilli* does not disclose or suggest all of the elements of the base claims. *Naumann* is cited solely as disclosing elements that are recited in the dependent claims listed above and does not cure the deficiencies noted in the combination of *Shin, Jones* and *Arimilli*. *Naumann* is directed to a scalable on-chip network that enables and manages data operations between multiple processing elements integrated on an integrated circuit or chip. Appellant respectfully submits that *Naumann* does not appear to disclose or suggest a hint signal that gives advance notification of a possible data transfer operation, the hint signal being transferred at least one data cycle prior to the transfer of associated data blocks. *Naumann* also does not appear to disclose or suggest control logic that generates the hint signal in response to the header block. Finally, *Naumann* does not appear to disclose or suggest a control block that responds to the hint signal by generating control signals to control the data transfer.

For at least the foregoing reasons, Appellant respectfully submits that the Examiner has not presented a *prima facie* case of obviousness against claims 2, 8, 9, 11, 12, 15, and 16. Accordingly, Appellant respectfully submits that pending claims 2, 8, 9, 11, 12, 15, and 16 are allowable over the cited references.

**CONCLUSION**

In view of the foregoing discussion, Appellant respectfully submits that the rejection of the pending claims 1-16 based on the *Shin*, *Jones*, *Arimilli* and *Naumann* references under 35 U.S.C. §103(a) is not proper. Accordingly, Appellant respectfully requests that the rejection of the pending claims 1-16 be overturned by the Board, and that the present patent application be allowed to issue as a patent with all pending claims.

Respectfully submitted,

Dated: November 13, 2008

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## VIII. APPEALED CLAIMS - APPENDIX

1. A system for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

a first circuit portion for providing said data blocks including said header block to a second circuit portion;

control logic associated with said second circuit portion for processing said header block and generating, in response to said header block, a hint signal that gives advance notification of a possible data transfer operation, said hint signal being operable to be transferred via a synchronizer at least one data cycle prior to the transfer of said data blocks to a third circuit portion; and

a control block associated with said third circuit portion, said control block operating responsive to said hint signal to generate data transfer control signals for controlling said third circuit portion in order to control output of said data blocks in a particular ordered grouping, wherein said first circuit portion,

said second circuit portion and said control logic are disposed in said first clock domain and said third circuit portion and said control block are disposed in said second clock domain.

2. The system for effectuating the transfer of data blocks including a header block as recited in claim 1, further comprising a synchronizer controller disposed between said first and second clock domains for providing at least one dead cycle control signal to said second circuit portion, wherein said at least one dead cycle control signal is indicative of the location of at least one dead cycle between said first and second clock signal.

3. The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said first circuit portion comprises a packet interface.

4. The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said second circuit portion comprises:

at least one queue operably coupled to said first circuit portion for temporarily storing said data blocks; and

a multiplexer (MUX) block operably coupled to said first circuit portion and said at least one queue, said MUX block operating under a MUX selection control signal generated by said control logic for selecting between data blocks stored in said at least one queue and data blocks provided by said first circuit portion without queuing, whereby said data blocks are transmitted as an output of said MUX block to said synchronizer.

5. The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said third circuit portion comprises means for selecting between data blocks directly transmitted by said synchronizer and data blocks buffered in said second clock domain, said means operating responsive to at least a portion of said data transfer control signals.

6. The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said header

block provides protocol control information relative to said data blocks.

7. The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein each of said data blocks comprises multiple bits.

8. The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said data blocks include at least one interval interleaved therein.

9. The system for effectuating the transfer of data blocks including a header block as recited in claim 1, wherein said data blocks comprise multi-channeled packet data, each channel's data blocks being interleaved with data blocks of other channels.

10. A method for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal (CLK1) and said second clock domain is operable with a second clock signal (CLK2), comprising:

processing a header block associated with data blocks that are to be sent from said first clock domain to said second clock domain via a synchronizer;

generating a hint signal that gives advance notification of a possible data transfer operation responsive to said header block and positioning said hint signal at least one cycle prior to the location of said data blocks, said processing said header block and said generating said hint signal being performed in said first clock domain;

transmitting said hint signal to a control block in said second clock domain, thereby indicating that said data blocks may be sent to receive circuitry in said second clock domain; and

generating appropriate control signals based on said hint signal for controlling output of said data blocks in a particular ordered grouping.

11. The method for effectuating the transfer of data blocks including a header block as recited in claim 10, further comprising:

generating advance notice indicative of the location of at least one dead cycle occurring between a first clock signal and a second clock signal used for transmitting data across a clock boundary;

receiving packet data and said advance notice indicative of the location of said at least one dead cycle;

calculating the optimal time to send said packet data relative to the location of said at least one dead cycle; and

transmitting ordered contiguous data blocks about said at least one dead cycle to a CLK1-to-CLK2 synchronizer for transmission to receive circuitry disposed in said second clock domain.

12. The method for effectuating the transfer of data blocks including a header block as recited in claim 11, wherein said at least one dead cycle comprises N - M dead cycles, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles such that $N/M > 1$.

13. A computer system having circuitry for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal (CLK1) and said second clock domain is operable with a second clock signal (CLK2), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

means for processing a header block associated with said data blocks to determine whether said data blocks may be sent from said first clock domain to said second clock domain via a synchronizer;

means for generating a hint signal that gives advance notification of a possible data transfer operation responsive to said header block wherein said hint signal is operable to be positioned at least one cycle prior to the possible location of said data blocks, said means for processing a header block and said means for generating a hint signal being disposed in said first clock domain; and

means for transmitting said hint signal to a control block in said second clock domain, thereby indicating that said data blocks may be sent to receive circuitry in said second clock domain, wherein said control block generates appropriate control signals

based on said hint signal for controlling output of said data blocks in a particular ordered grouping.

14. The computer system as recited in claim 13, further comprising a multiplexer (MUX) block disposed in said second clock domain for operating responsive to at least a portion of said control signals.

15. The computer system as recited in claim 13, further comprising means for determining where a dead cycle occurs between said first and second clock signals.

16. The computer system as recited in claim 15, further comprising means for optimizing the position of said data blocks relative to said dead cycle.

## IX. EVIDENCE - APPENDIX

None.

## X. RELATED PROCEEDINGS - APPENDIX

None.